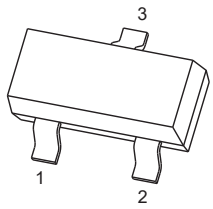
IRLML6401

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

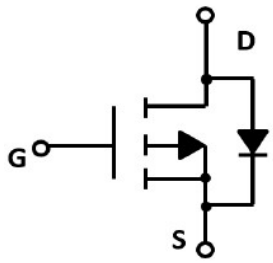
$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
-12V	50 mΩ@4.5V	-4.3A
	85 mΩ@2.5V	
	30mΩ@1.8V	

SOT-23



1. GATE
2. SOURCE
3. DRAIN

Schematic diagram



General Description

- Trench Power LV MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge

Applications

- PWM applications
- Power management
- Load switch

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-12	V
Gate-source Voltage		V_{GS}	±10	V
Drain Current	T_A=25℃	I_D	-4.3	A
	T_A=70℃		-3	
Pulsed Drain Current [A]		I_{DM}	-15	A
Total Power Dissipation	T_A=25℃	P_D	1	W
	T_A=70℃		0.64	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	125	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
IRLML6401	F2	1F/F****	3000	45000	180000	7“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-12			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-19V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.4	-0.62	-0.95	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-3.8A		36	50	mΩ
		V_{GS}=-2.5V, I_D=-3.0A		55	85	
Diode Forward Voltage	V_{SD}	I_S=-3.8A,V_{GS}=0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHZ		606		pF
Output Capacitance	C_{oss}			114		
Reverse Transfer Capacitance	C_{rss}			103		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-10V,I_D=-3.8A		8.48		nC
Gate-Source Charge	Q_{gs}			1.54		
Gate-Drain Charge	Q_{gd}			2.61		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V, V_{DS}=-10V, I_D=-3.8A R_{GEN}=3Ω		5.8		
Turn-on Rise Time	t_r			34.8		
Turn-off Delay Time	$t_{D(off)}$			51.4		
Turn-off fall Time	t_f			52		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

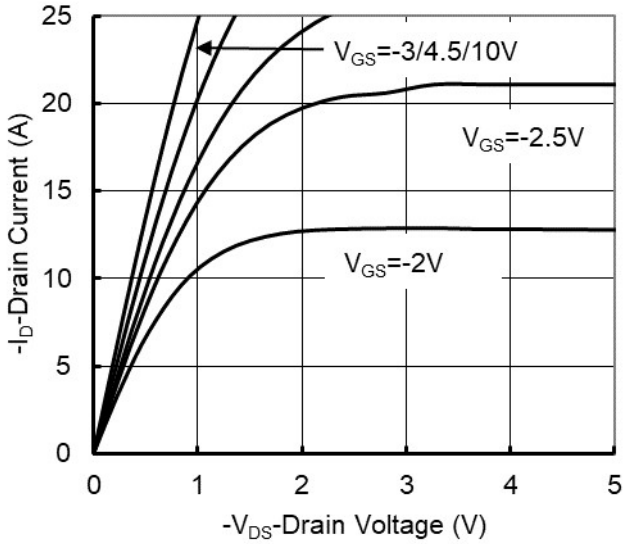


Figure1. Output Characteristics

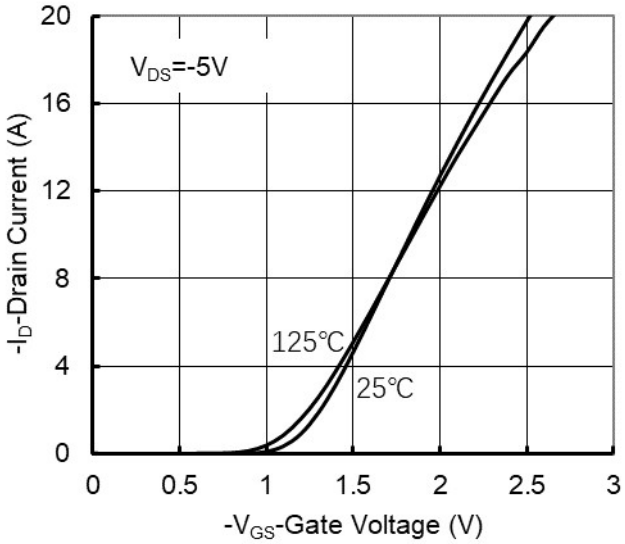


Figure2. Transfer Characteristics

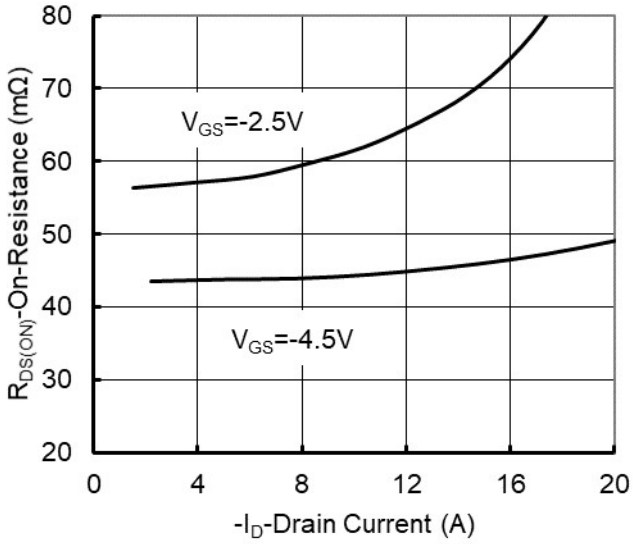


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

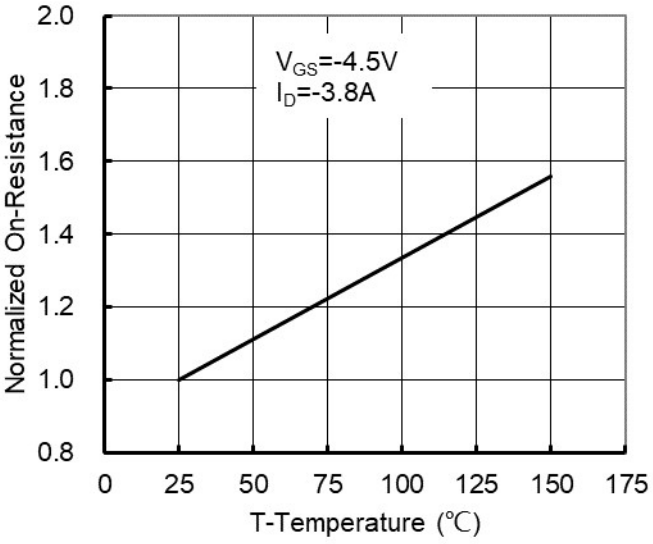


Figure 4: On-Resistance vs. Junction Temperature

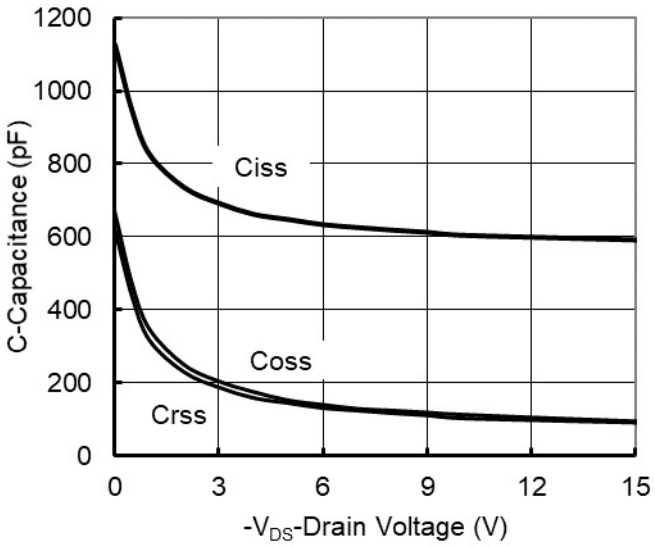


Figure5. Capacitance Characteristics

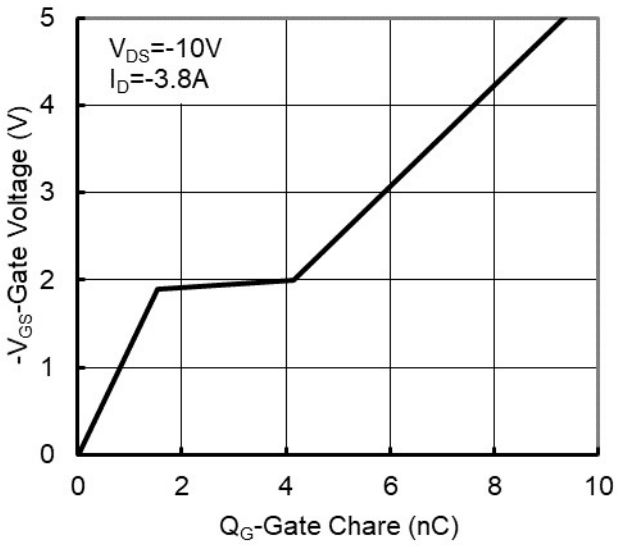


Figure6. Gate Charge

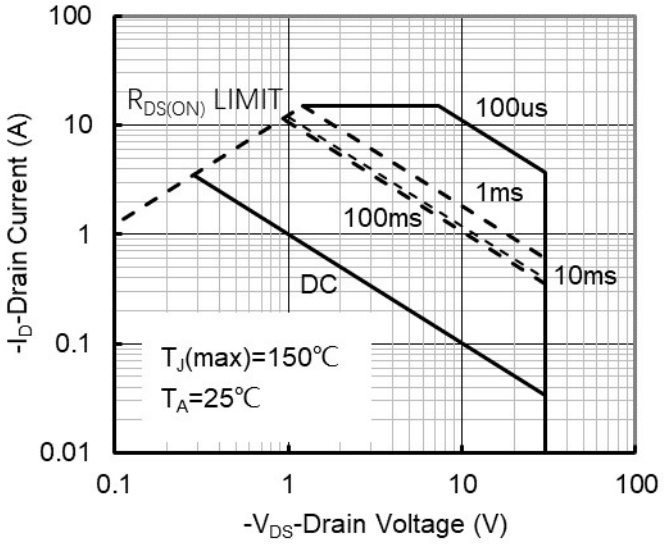


Figure7. Safe Operation Area

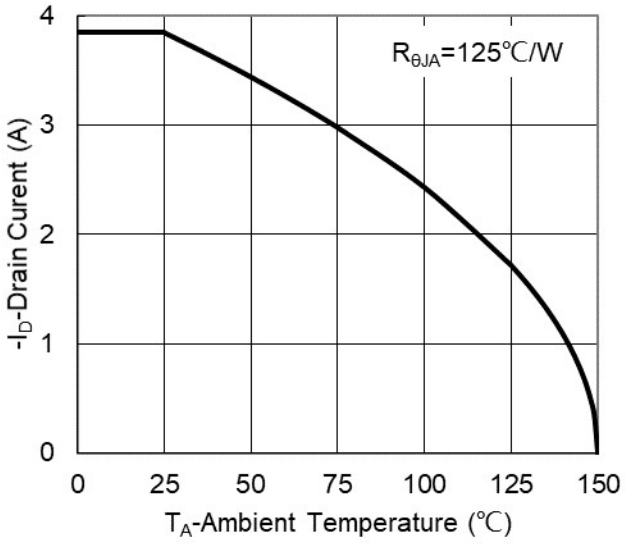


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

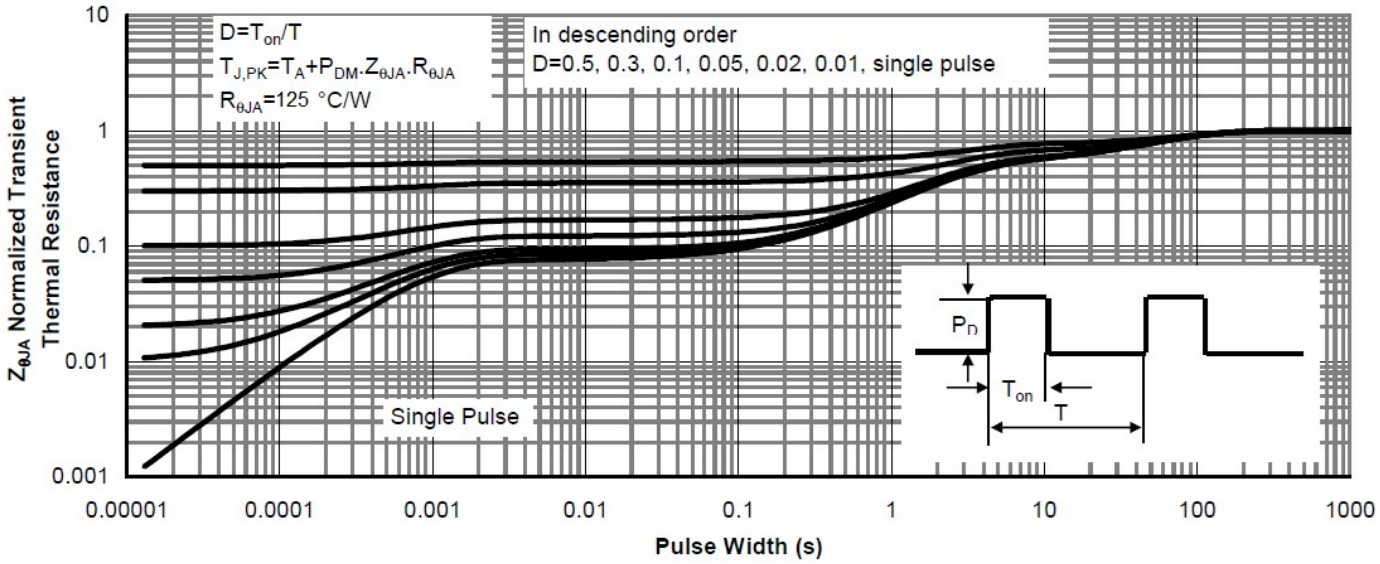
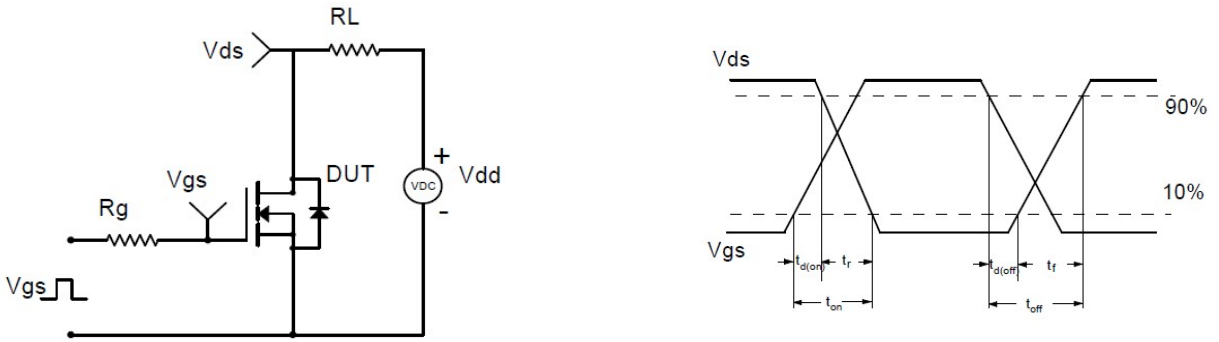
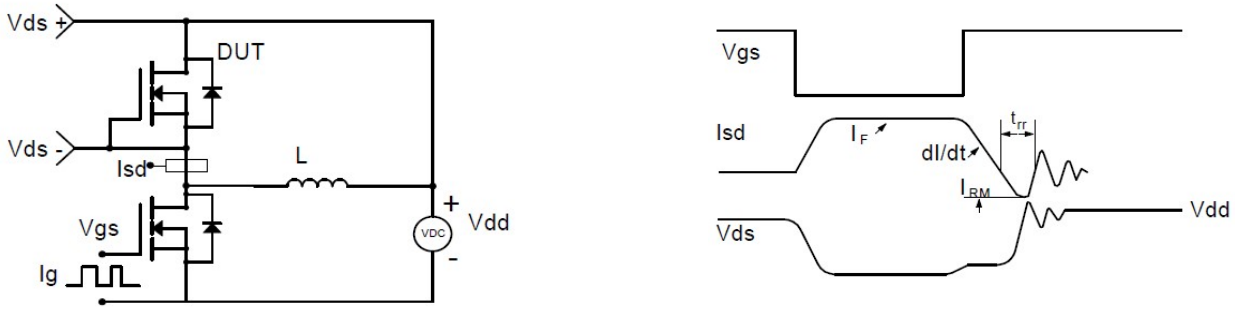


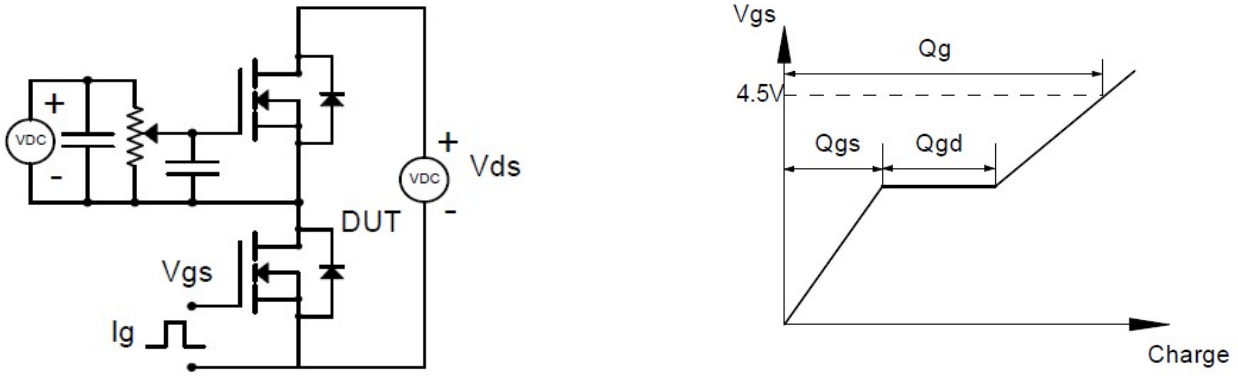
Figure9. Normalized Maximum Transient Thermal Impedance



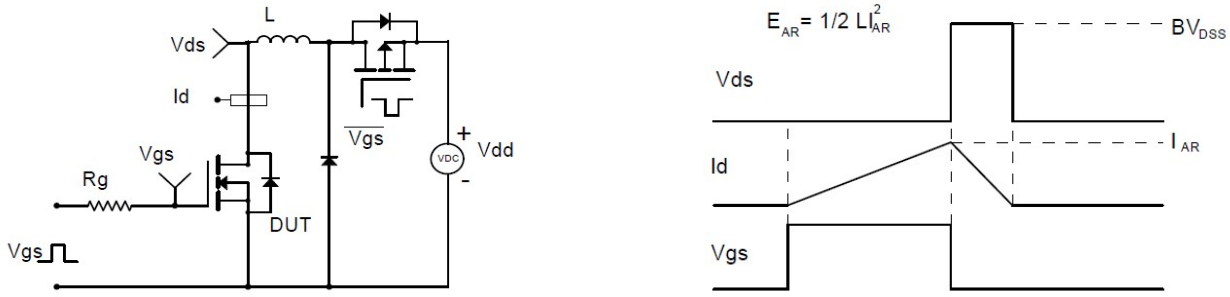
Resistive Switching Test Circuit & Waveforms



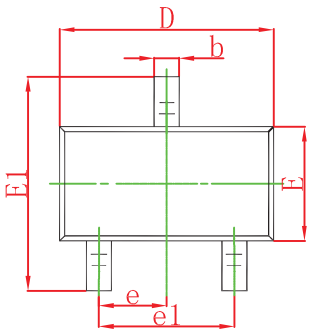
Diode Recovery Test Circuit & Waveforms

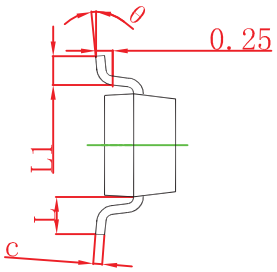


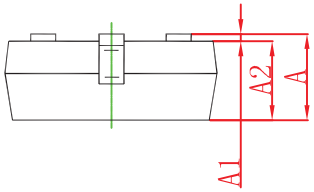
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

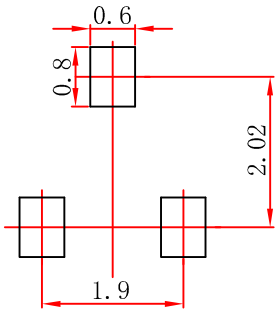






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.