

# Dual 2-Input Exclusive-OR Gate

## NL27WZ86

The NL27WZ86 is a high performance dual 2-input Exclusive-OR Gate operating from a 1.65 V to 5.5 V supply.

### Features

- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- 2.9 ns  $t_{PD}$  at  $V_{CC} = 5$  V (typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- $I_{OFF}$  Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in US8, UDFN8 and UQFN8 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

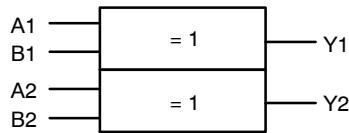


Figure 1. Logic Symbol



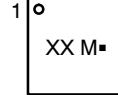
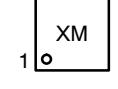
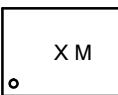
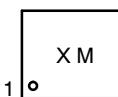
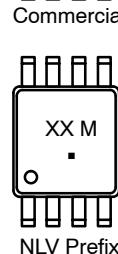
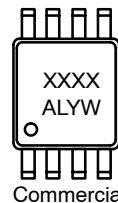
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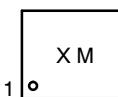
### MARKING DIAGRAMS



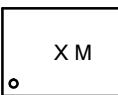
**US8**  
**US SUFFIX**  
**CASE 493**



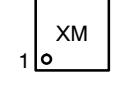
**UDFN8, 1.45x1.0**  
**MU3 SUFFIX**  
**CASE 517BZ**



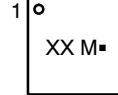
**UDFN8, 1.95x1.0**  
**MU1 SUFFIX**  
**CASE 517CA**



**UQFN8, 1.4x1.2**  
**MQ2 SUFFIX**  
**CASE 523AS**



**UQFN8, 1.6x1.6**  
**MQ1 SUFFIX**  
**CASE 523AN**



X, XX, XXXX	= Specific Device Code
A	= Assembly Location
L	= Lot Code
Y	= Year Code
W	= Week Code
M	= Date Code
▪	= Pb-Free Package

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

# NL27WZ86

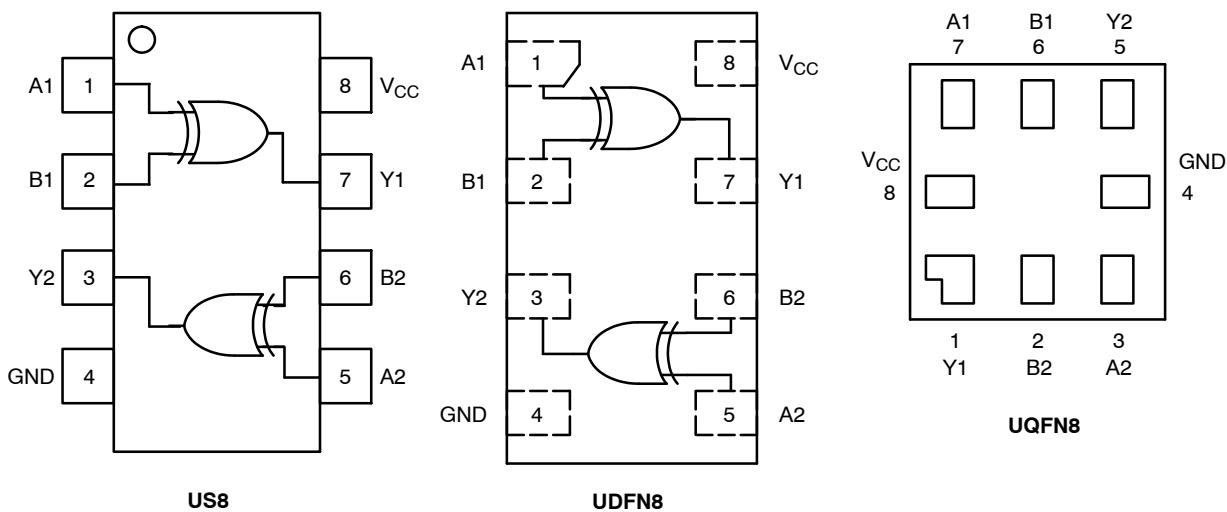


Figure 2. Pinout

## PIN ASSIGNMENT (US8 / UDFN8)

Pin	Function
1	A1
2	B1
3	Y2
4	GND
5	A2
6	B2
7	Y1
8	V <sub>CC</sub>

## PIN ASSIGNMENT (UQFN8)

Pin	Function
1	Y1
2	B2
3	A2
4	GND
5	Y2
6	B1
7	A1
8	V <sub>CC</sub>

## FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

## MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
$V_{CC}$	DC Supply Voltage	NLV -0.5 to +7.0 -0.5 to +6.5	V
$V_{IN}$	DC Input Voltage	NLV -0.5 to +7.0 -0.5 to +6.5	V
$V_{OUT}$	DC Output Voltage (NLV) Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +7.0 -0.5 to +7.0	V
	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-50	mA
$I_{OK}$	DC Output Diode Current $V_{OUT} < GND$	-50	mA
$I_{OUT}$	DC Output Source/Sink Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC Supply Current per Supply Pin or Ground Pin	$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 secs	260	°C
$T_J$	Junction Temperature Under Bias	+150	°C
$\theta_{JA}$	Thermal Resistance (Note 2)	US8 UQFN8 UDFN8 250 210 231	°C/W
$P_D$	Power Dissipation in Still Air	US8 UQFN8 UDFN8 500 595 541	mW
MSL	Moisture Sensitivity	Level 1	-
$F_R$	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
$V_{ESD}$	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model 2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)	$\pm 100$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	1.65	5.5	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	0	$V_{CC}$	
		0	5.5	
$T_A$	Operating Temperature Range	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time $V_{CC} = 1.65$ V to 1.95 V $V_{CC} = 2.3$ V to 2.7 V $V_{CC} = 3.0$ V to 3.6 V $V_{CC} = 4.5$ V to 5.5 V	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-55°C ≤ T <sub>A</sub> ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		1.65 to 1.95	0.65 V <sub>CC</sub>	–	–	0.65 V <sub>CC</sub>	–	V
			2.3 to 5.5	0.70 V <sub>CC</sub>	–	–	0.70 V <sub>CC</sub>	–	
V <sub>IL</sub>	Low-Level Input Voltage		1.65 to 1.95	–	–	0.35 V <sub>CC</sub>	–	0.35 V <sub>CC</sub>	V
			2.3 to 5.5	–	–	0.30 V <sub>CC</sub>	–	0.30 V <sub>CC</sub>	
V <sub>OH</sub>	High-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -100 µA I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -16 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V <sub>CC</sub> - 0.1 1.29 1.4 2.1 2.2 2.4 2.7 3.8	V <sub>CC</sub> – – – – – – –	– – – – – – – –	V <sub>CC</sub> - 0.1 1.29 1.9 2.2 2.4 2.3 3.8	– – – – – – –	V
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 100 µA I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	– – – – – –	– 0.08 0.2 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55	– – – – – – –	0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	1.65 to 5.5	–	–	±0.1	–	±1.0	µA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V	0	–	–	1.0	–	10	µA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	–	–	1.0	–	10	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

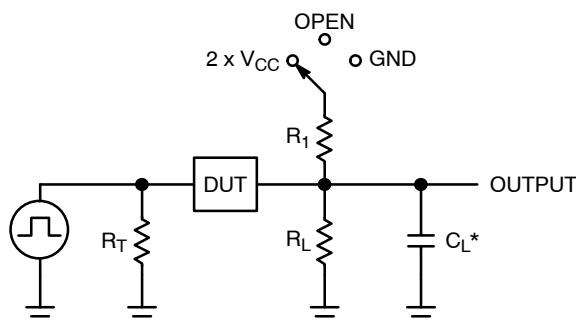
## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55 to 125°C		Units
				Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, (A or B) to Y	1.65 to 1.95	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 MΩ R <sub>1</sub> = Open	–	7.9	9.0	–	10.5	ns
		2.3 to 2.7		–	4.1	7.0	–	7.5	
		3.0 to 3.6		–	3.0	4.8	–	5.2	
		4.5 to 5.5		–	2.2	3.5	–	3.8	
		3.0 to 3.6	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, R <sub>1</sub> = Open	–	3.8	5.4	–	5.9	
		4.5 to 5.5		–	2.9	4.2	–	4.6	

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	2.5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	2.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub> 10 MHz, V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V or V <sub>CC</sub>	9 11	pF

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.



$C_L$  includes probe and jig capacitance

$R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )

$f = 1$  MHz

Figure 3. Test Circuit

Test	Switch Position	$C_L$ , pF	$R_L$ , $\Omega$	$R_1$ , $\Omega$
$t_{PLH} / t_{PHL}$	Open	See AC Characteristics Table		
$t_{PLZ} / t_{PZL}$	$2 \times V_{CC}$	50	500	500
$t_{PHZ} / t_{PZH}$	GND	50	500	500

X = Don't Care

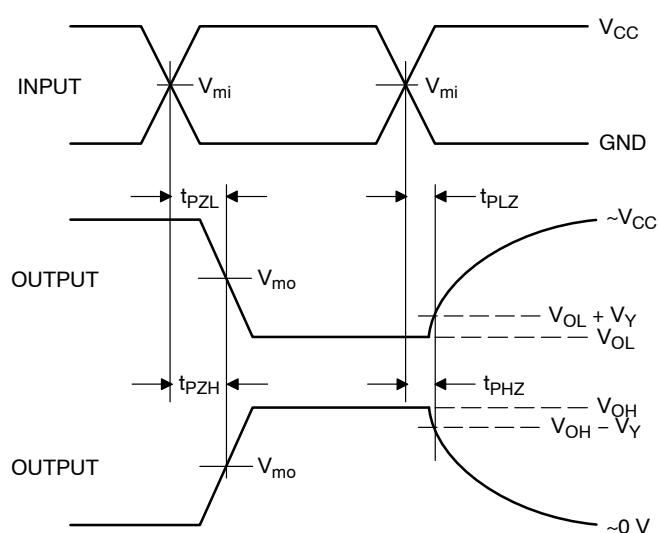
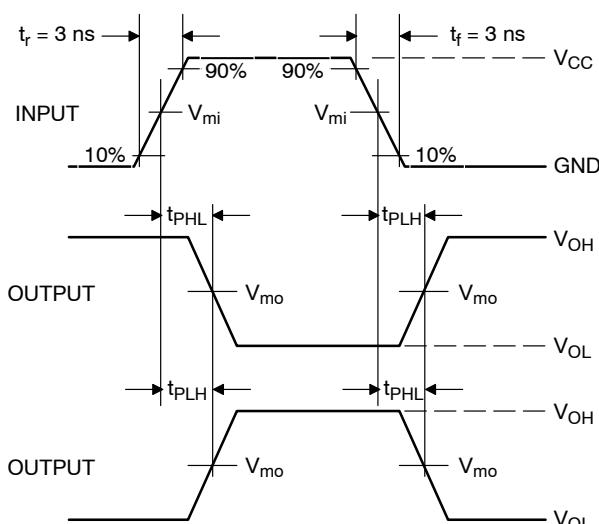


Figure 4. Switching Waveforms

$V_{CC}$ , V	$V_{mi}$ , V	$V_{mo}$ , V		$V_Y$ , V
		$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

# NL27WZ86

## DEVICE ORDERING INFORMATION

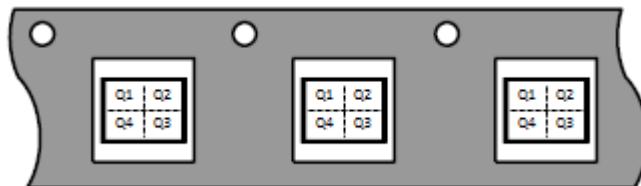
Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping <sup>†</sup>
NL27WZ86USG	US8	L8	Q4	3000 / Tape & Reel
NLV27WZ86USG*	US8	L8	Q4	3000 / Tape & Reel
NL27WZ86MQ1TCG	UQFN8, 1.6 x 1.6, 0.5P	AC	Q1	3000 / Tape & Reel
NL27WZ86MU1TCG (In Development)	UDFN8, 1.95 x 1.0, 0.5P	TBD	TBD	3000 / Tape & Reel
NL27WZ86MU3TCG (In Development)	UDFN8, 1.45 x 1.0, 0.35P	TBD	TBD	3000 / Tape & Reel
NL27WZ86MQT2CG (In Development)	UQFN8, 1.4 x 1.2, 0.4P	TBD	TBD	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

## Pin 1 Orientation in Tape and Reel

### Direction of Feed



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

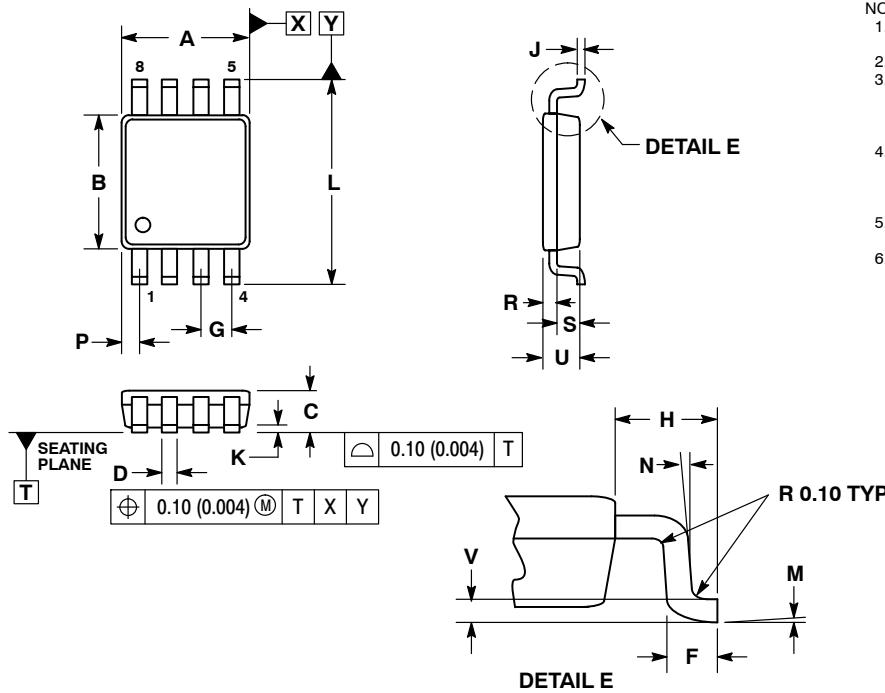
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SCALE 4:1

US8  
CASE 493  
ISSUE D

DATE 15 JUL 2015

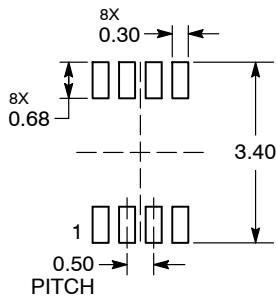


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203MM (0.003-0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED  $\pm 0.0508\text{MM}$  (0.002").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

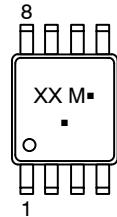
### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code  
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.

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DESCRIPTION:	US8	PAGE 1 OF 1

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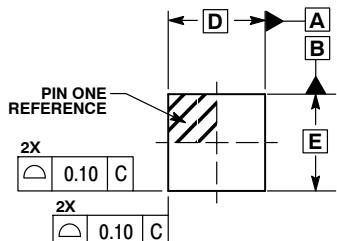
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

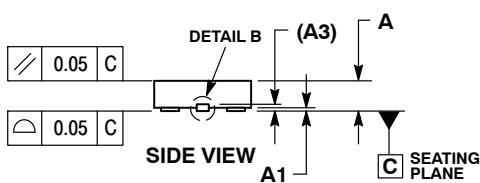
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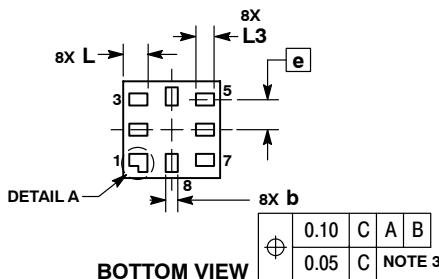
SCALE 4:1



TOP VIEW



SIDE VIEW A1



BOTTOM VIEW

UQFN8, 1.6x1.6, 0.5P  
CASE 523AN-01  
ISSUE O

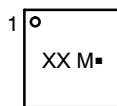
DATE 26 NOV 2008

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
L	0.35	0.45
L1	---	0.15
L3	0.25	0.35

GENERIC  
MARKING DIAGRAM\*



XX = Specific Device Code

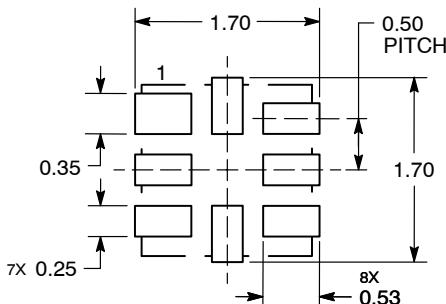
M = Date Code

■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

Pb-Free indicator, "G" or microdot "■", may or may not be present.

SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	8 PIN UQFN, 1.6X1.6, 0.5P	PAGE 1 OF 1

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